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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/961,172	09/24/2001	Kazuhito Higuchi	214318US2S	8217

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EXAMINER	
TRAN, THANH Y	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 07/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/961,172	KAZUHITO HIGUCHI	
	Examiner	Art Unit	
	Thanh Y. Tran	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the c rrespondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/24/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of species Group I, Embodiment 1 including claims 1-4 in Paper No. 02/28/04 is acknowledge. The traversal is on the ground(s) that "a search and examination of the entire application would not place a serious burden on the Examiner". This is not found persuasive because the inventions are divergent subject matters and the search for a method of manufacturing a circuit device in Group I is not required the same search in Group II, and a method of manufacturing a circuit device with bonding step of press a terminal section against a wiring substrate in Embodiment 1 is not required the same search in Embodiment 2.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-2 and 4 are rejected under 35 U.S.C. 102(e) as being anticipated by Fukatsu et al (U.S. 6,528,870).

As to claim 1, Fukatsu et al discloses in figure 3B, an apparatus and a corresponding method for manufacturing a circuit device, comprising: a bonding step of

pressing a terminal section (see a nearest electronic component having terminal section (pattern 33) mounted on the surface of wiring layer 42 of base board 41) of an electronic component including an element (36) for performing an electrical function against a wiring substrate (41) having a wiring layer (42) by a tool (46) whose pressing face has a given shape to electrically bond the electronic component and the wiring layer (42) together at the terminal section (33); and a stacking step of electrically bonding another component (see the upper stackable electronic component mounted above the nearest electronic component as shown in figure 3B) to at least part of the terminal section (33) bonded by the tool (46).

As to claim 2, Fukatsu et al discloses in figure 3B, an apparatus and a corresponding method for manufacturing a circuit device, wherein all terminal sections (33) of electronic components have substantially same height (see terminal sections 33 on the left side and right side of the electronic components as shown in figure 3B, they have the substantially same height).

As to claim 4, Fukatsu et al discloses in figure 3B, an apparatus and a corresponding method for manufacturing a circuit device, wherein all terminal sections (33) of electronic components have substantially same height (see terminal sections 33 on the left side and right side of the electronic components as shown in figure 3B, they have the substantially same height).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fukatsu et al (U.S. 6,528,870) in view of Tsukahara (U.S. 6,051,093).

As to claim 3, Fukatsu et al discloses in figure 3B, an apparatus and a corresponding method for manufacturing a circuit device, comprising: a bonding step of mounting an electronic component including an element (36) for performing an electrical function on a wiring layer (42) of a wiring substrate (41) and pressing a terminal section (33) of the mounted electronic component against the wiring substrate (41) by a tool (46) whose pressing face has a given shape to electrically bond the electronic component and the wiring layer (42) together at the terminal section (33); and a stacking step of electrically bonding another component (see Fig. 3B, another component is the upper stackable electronic component mounted above the nearest electronic component (as mentioned in claim 1)) to at least part of the terminal section (33) bonded by the tool (46).

Fukatsu et al does not teach a bonding step of mounting an electronic component including an element for performing an electrical function on an insulation layer stacked on a wiring layer.

Tsukahara discloses in figures 14a-14c an apparatus and a corresponding method, comprising a bonding step of mounting an electronic component (1) including an element (2) for performing an electrical function on an insulation layer (21) stacked on a wiring layer (see wiring layer 5 as indicated at figure 14a). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to

modify the apparatus of Fukatsu et al by including an insulation layer which is stacked on a wiring layer as taught by Tsukahara for the purpose of protecting the active surface of electronic component and surface of electrode so as to increase the reliability of connection when the tool (suction nozzle) is heated and pressed (see Figs. 14a-14c, col. 8, line 61 – col. 9., line 5 in Tsukahara).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tottori et al (U.S. 5,394,608) teaches Laminated semiconductor device and fabricating method thereof.

Muramatsu et al (U.S. 6,420,664) teaches Metal foil having bumps, circuit substrate having the metal foil, and semiconductor device having the circuit substrate.

Nakamura et al (U.S. 6,476,467) teaches semiconductor device and process for producing the same.

Fujimoto et al (U.S. 5,115,545) teaches Apparatus for connecting semiconductor devices to wiring boards.

Toyosawa (U.S. 6,552,419) teaches semiconductor device and liquid crystal module using the same.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on Monday through Thursday and on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo, can be reached on (571) 272-1957. The fax phone number for the organization where this application or proceeding is assigned is (703) 305-3431.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

TYT

David A. Zarneke
Primary Exam
6/26/04